

UNITED STATES PATENT AND TRADEMARK OFFICE  
**CERTIFICATE OF CORRECTION**

PATENT NO. : 7,557,406 B2  
APPLICATION NO. : 11/707406  
DATED : July 7, 2009  
INVENTOR(S) : Parthasarathy et al.

Page 1 of 1

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 4, Lines 40-46 reads:

“In one embodiment, for a 2mm × 2mm die with 60μm high pillars, adequate stress relief is provided in a HVFET with an on-resistance of about 10ohm utilizing a layout comprising four racetrack transistor sections separated by dummy silicon pillars, each having a pitch (y-direction) of about 13μm and a length (x-direction) of about 450μm.”

It should read:

“In one embodiment, for a 2mm × 2mm die with 60μm high pillars, adequate stress relief is provided in a HVFET with an on-resistance of about 1 ohm utilizing a layout comprising four racetrack transistor sections separated by dummy silicon pillars, each having a pitch (x-direction) of about 13μm and a length (y-direction) of about 450μm.”

Signed and Sealed this  
Thirty-first Day of July, 2012

A handwritten signature in black ink that reads "David J. Kappos". The signature is written in a cursive, flowing style with a large initial 'D' and a stylized 'K'.

David J. Kappos  
*Director of the United States Patent and Trademark Office*